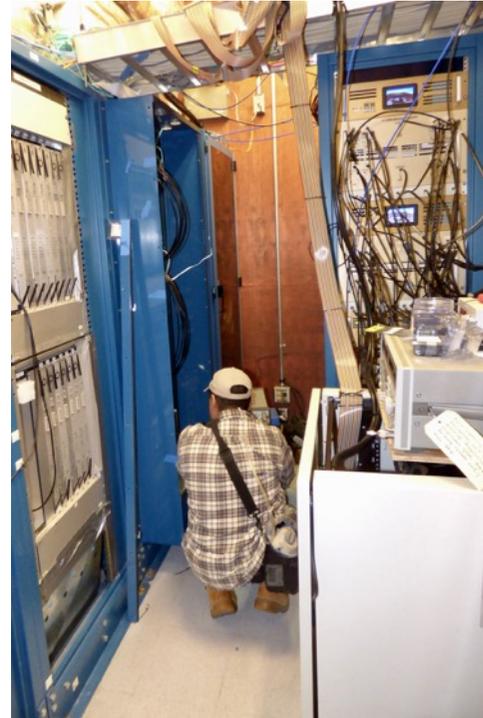# SWARM: current status & a bright future. . .
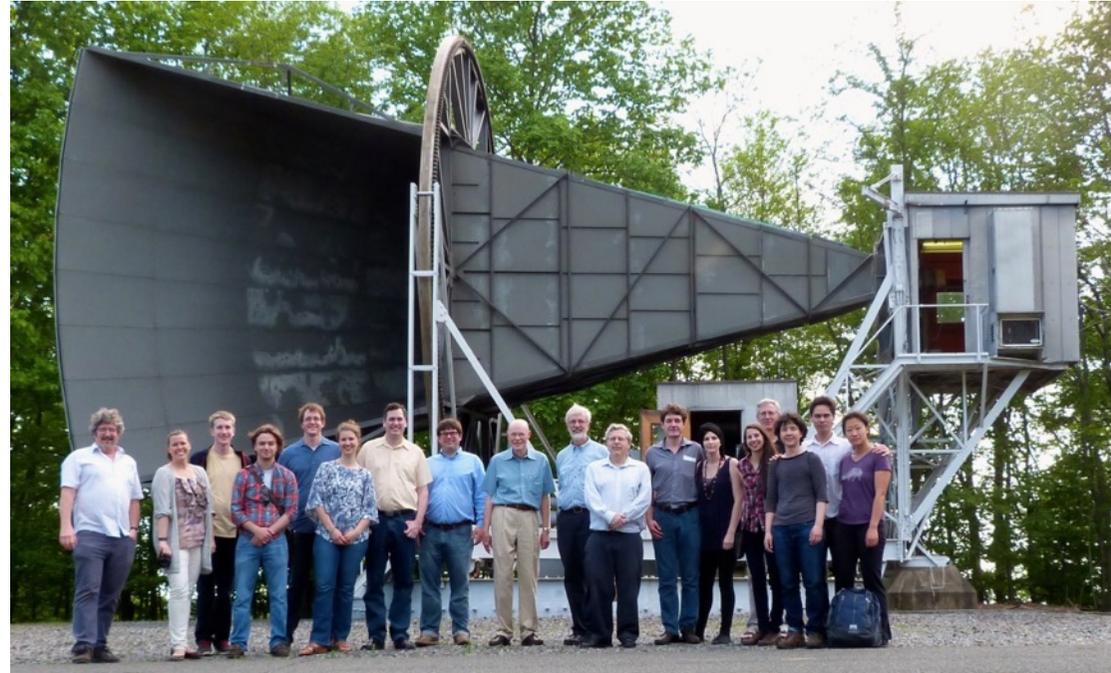

Jonathan Weintroub
for the SWARM Development Team
SMA Science in the Next Decade, ASIAA, Taiwan
27 October 2016

. . .or:

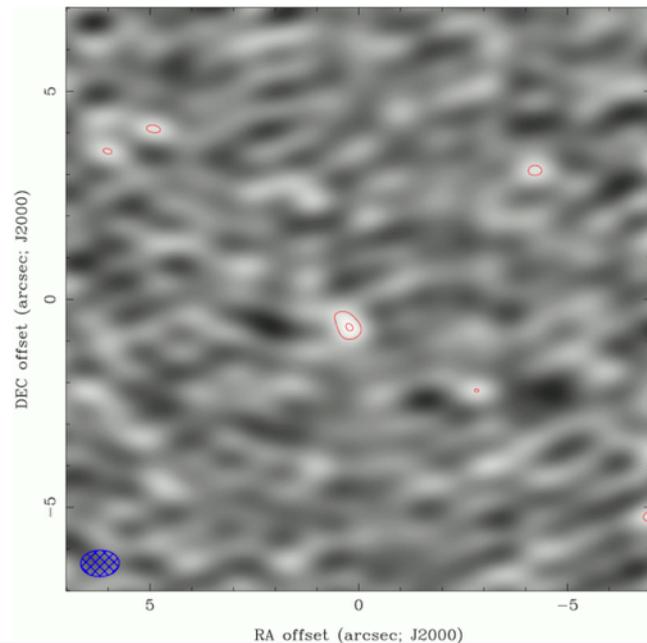## Behold the Power of SWARM

Glen

Category: General

Antennas: 1,3,4,5,6,7,8

entered by: gpetitpa

LO Frequency: 343 GHz
RMS: 0.49 mJy (contours=3,4,5 sigma)
Beam=0.92x0.63"

...ack taken in dual-rx SWARM-only mode on Sunday night. The tau ...ne phase was OK considering we are in EXT. Both the 345s and ...z USB (LO = 343 GHz). The pointing on Antenna 7 was poor, and ...es, the 400s on Antenna 7 were basically unusable.

...ugh the calibration I find that the rms of *each* 6 GHz wide ...s around 1 mJy when I image them individually (the 400 images ...i the flagging of Antenna 7). Combining all the data into a full ...a **dirty map with an rms of 0.55 mJy (550 uJy!)**.

...ertain because Uranus was resolved on most baselines and I did ...I assumed a scale factor of '1' for baselines with no useful Uranus ...I scale factors of 1-1.3, and I am not 100% certain that the tsys ...od as it used to be for ASIC.

The target (as calibrated) has a flux of 2.35 mJy and is detected at the 4.3 sigma level. This would have been around a 2.5 sigma detection with just the ASIC.

For comparison, the online sensitivity calculator (assuming 1 mm PWV) gives 1.93 m Jy per 2...

Shed a tear . . .

The ASIC correlator was shut down about a week ago, it served SMA well
(presentation time is far too valuable for a minute of silence)
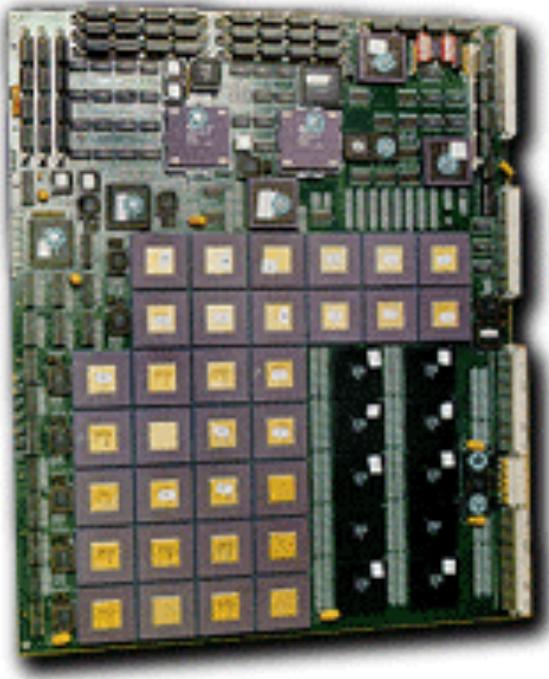
Mark 4 XF 'CB'
(Canaris ASIC from late 1990's)

90 CBs in system
32 ASICs/CB = 2880 ASICs/system

~25 kW digital+analog+cooling

IF downconverter and sampler assembly (C2DC)

8 antennas x 6 'blocks' x 2 pols = 96 assemblies

96 x 4 chunks/block
= 384 IF channels and ADCs

- Highly hybridized, 4 GHz band divided into 48 'chunks' per antenna.
- SMA ASIC was XF architecture, in common with many others, including ALMA
- We now strongly favor FX architecture, supported by FPGA DSP technology.

ASIAA 5 GSa/s sampler is foundational wideband technology

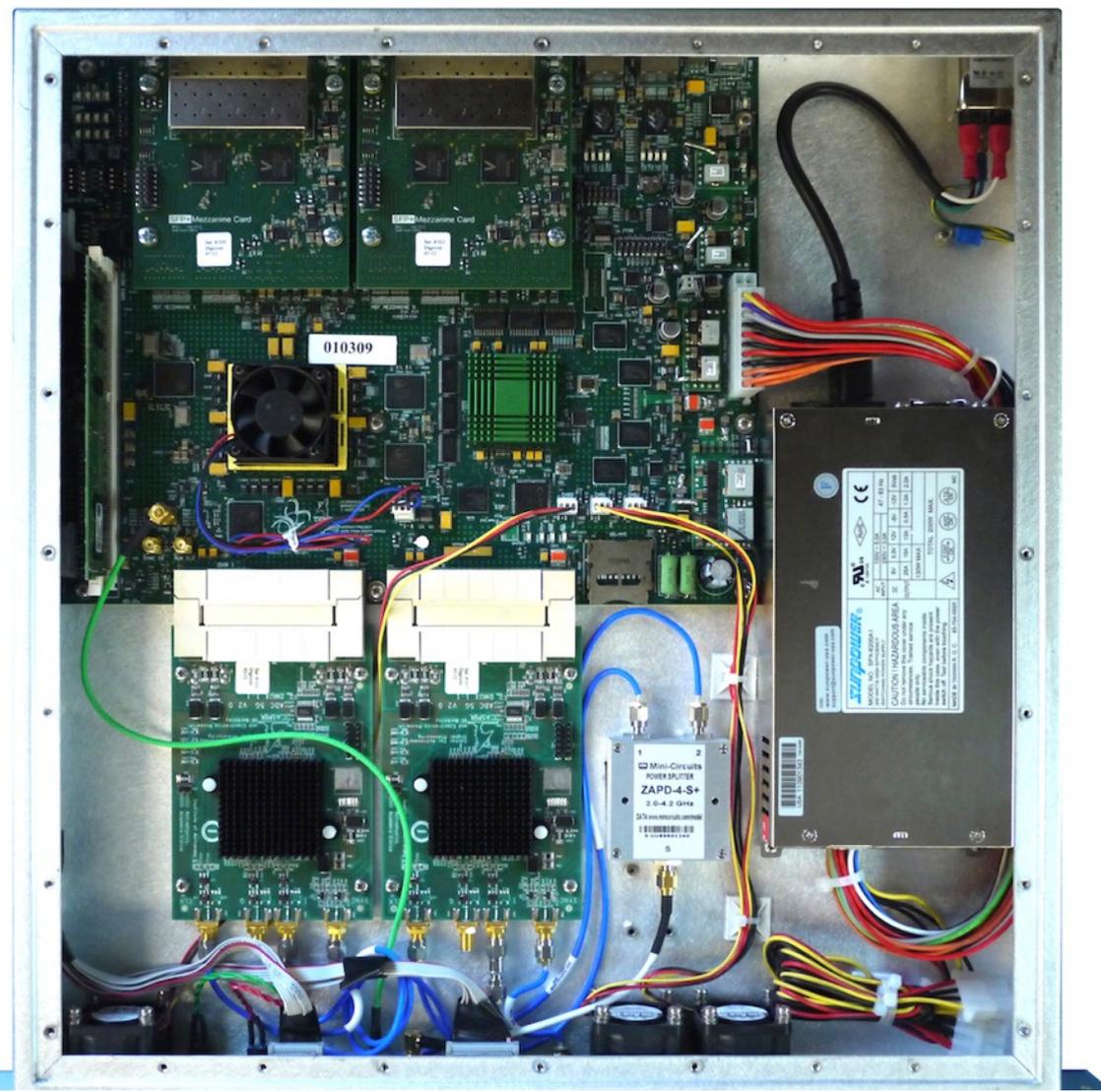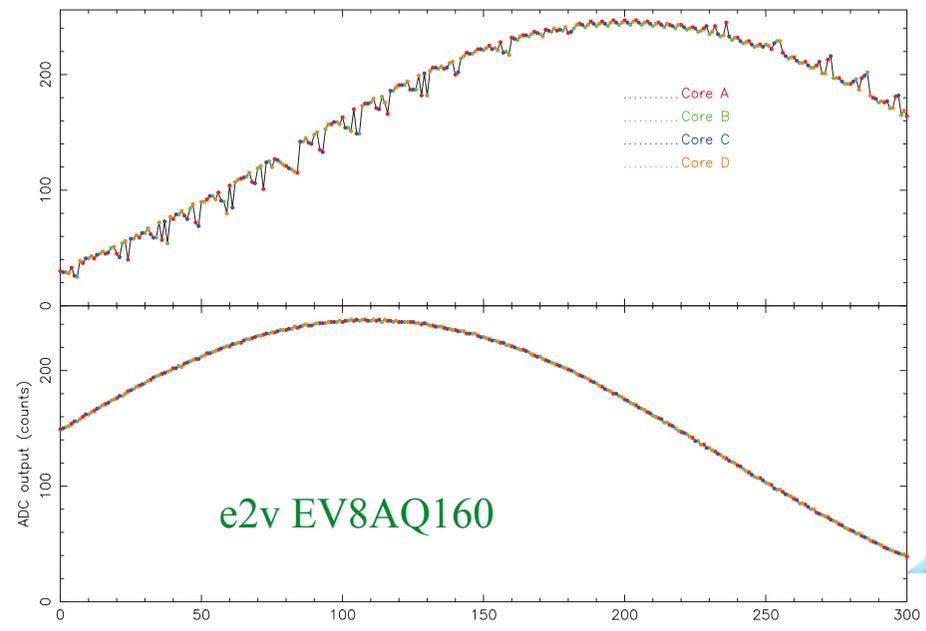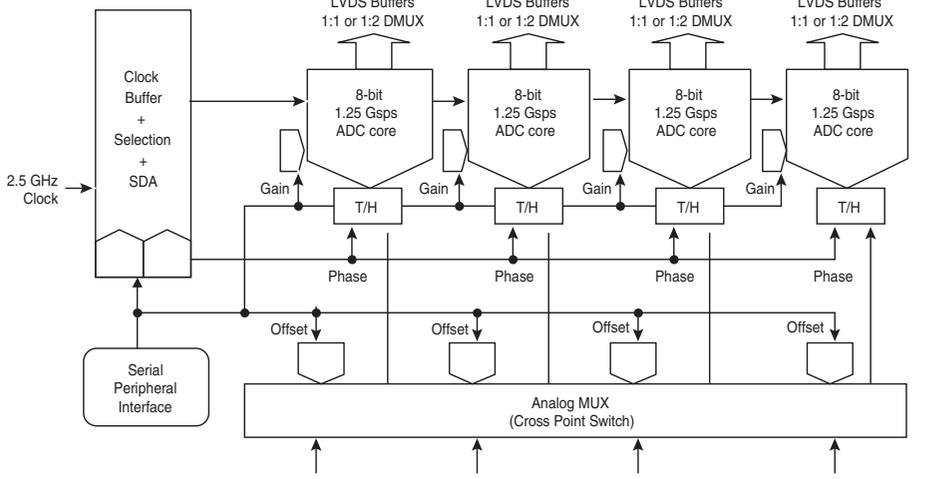**(Jiang et al., PASP 126, 761; 2014; Patel et al., JAI 3, 1 2014)**

Ultra Fast Analog-to-Digital Converters are typically interleaved multi-core devices
This introduces interleaving artifacts which must be calibrated

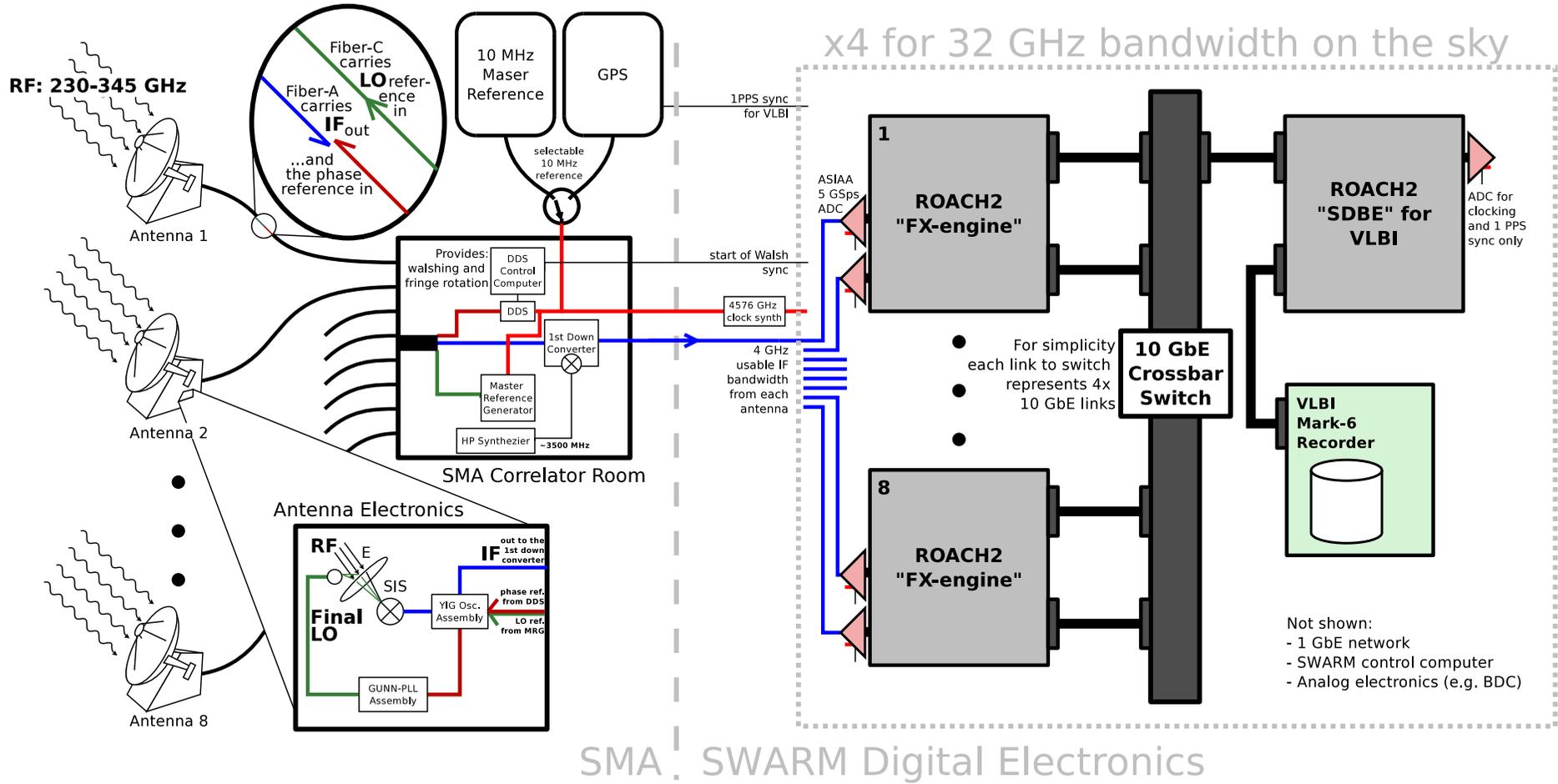CASPER ROACH2 with Dual ASIAA ADCs
as configured for SWARM
Photo by Derek Kubo

e2v EV8AQ160

(For more on CASPER see Hickish et al., JAI, 2016, in review)

# SWARM: SMA Wideband Astronomical ROACH2 Machine

(Primiani et al., JAI, 2016, in review)

1 "quadrant": 2 GHz per receiver per sideband = 8 GHz; 32 GHz total

Benefits relative to ASIC correlator:

1. high uniform spectral resolution with no sacrifice of bandwidth,
2. smaller footprint and power consumption.
3. better digital efficiency with 4-bit cross-correlation
4. 2 GHz wide bands easier to reduce, result in higher quality spectra
5. Natively supports VLBI phasing and recording, 16 Gbps/quadrant
6. Built with COTS components
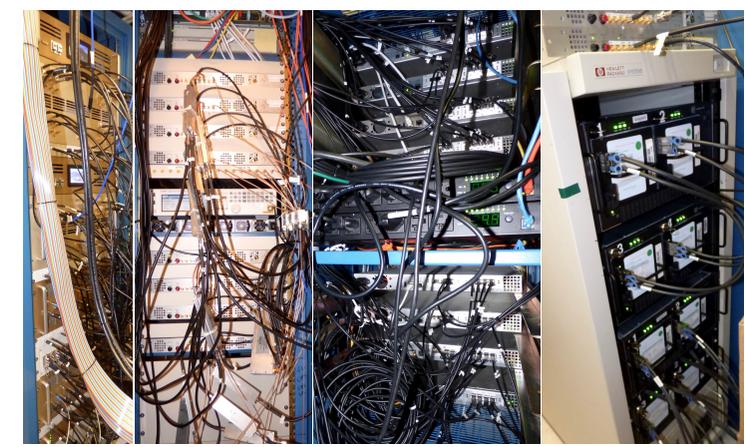
"FGPA Utilization": fine spectral resolution requires large FFTs

will all the SWARM logic fit?

(Primiani, Weintroub, deWerd, 2011,

https://www.cfa.harvard.edu/twpub/SMAwideband/MemoSeries/sma_wideband_utilization_1.pdf **)**
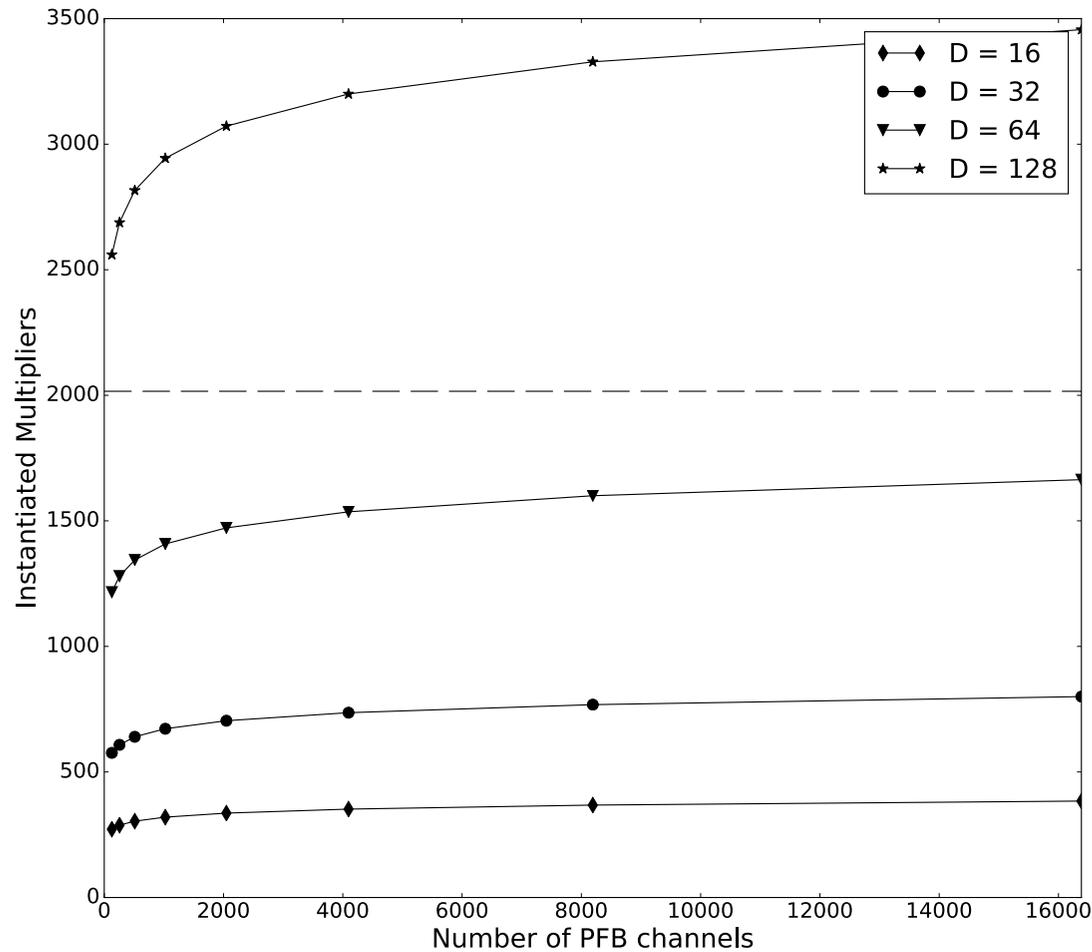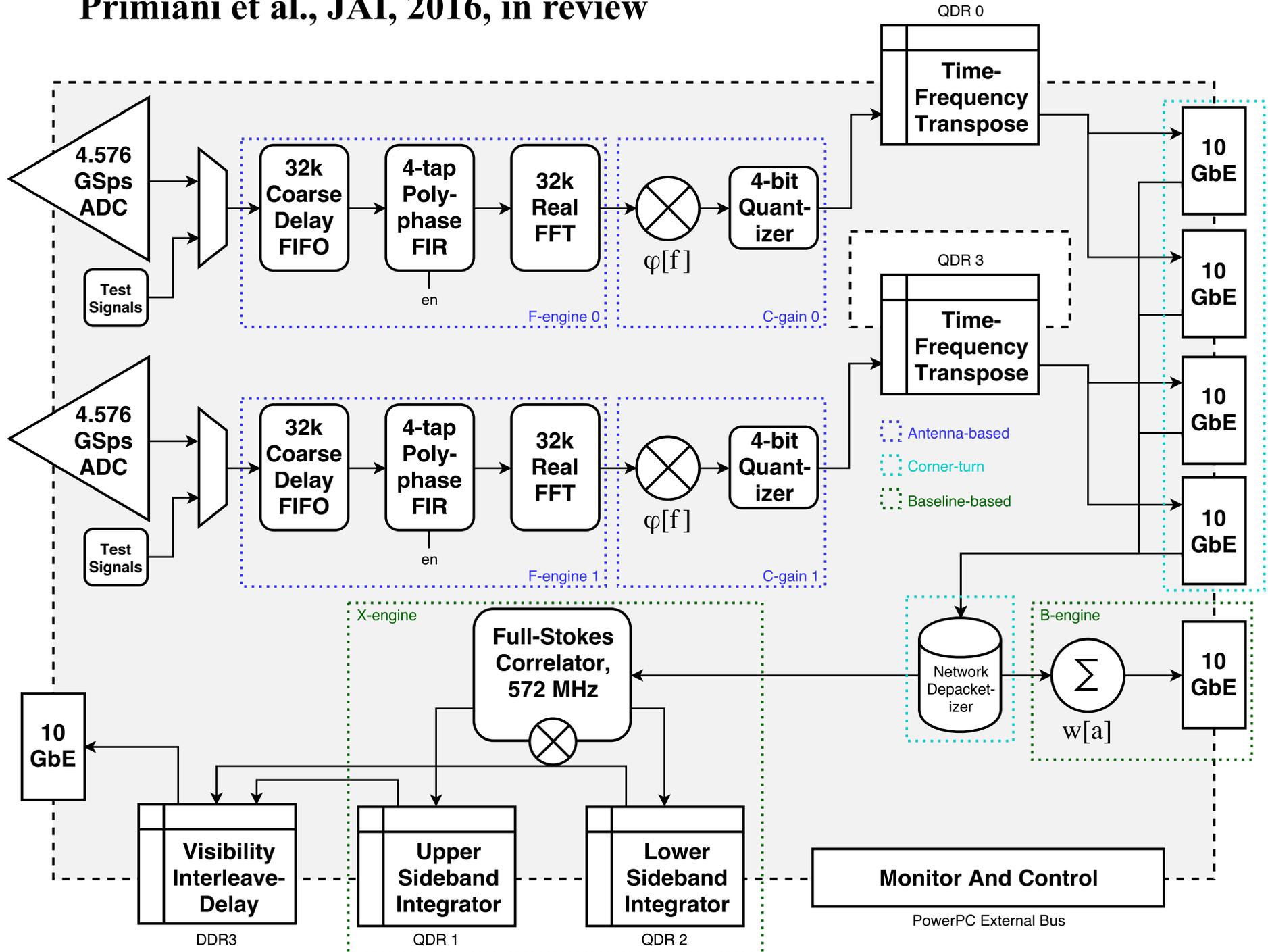

$$M_{\text{PFB}} = \underbrace{D \log_2 ND}_{\text{FFT}} + \underbrace{TD}_{\text{FIR}} - \underbrace{2D}_{\text{optimization}}$$

Example calculation of "instantiated multipliers" needed in FPGA for large "polyphase filterbank" (a type of FFT with improved isolation)

SWARM FPGA logic subsumes great complexity
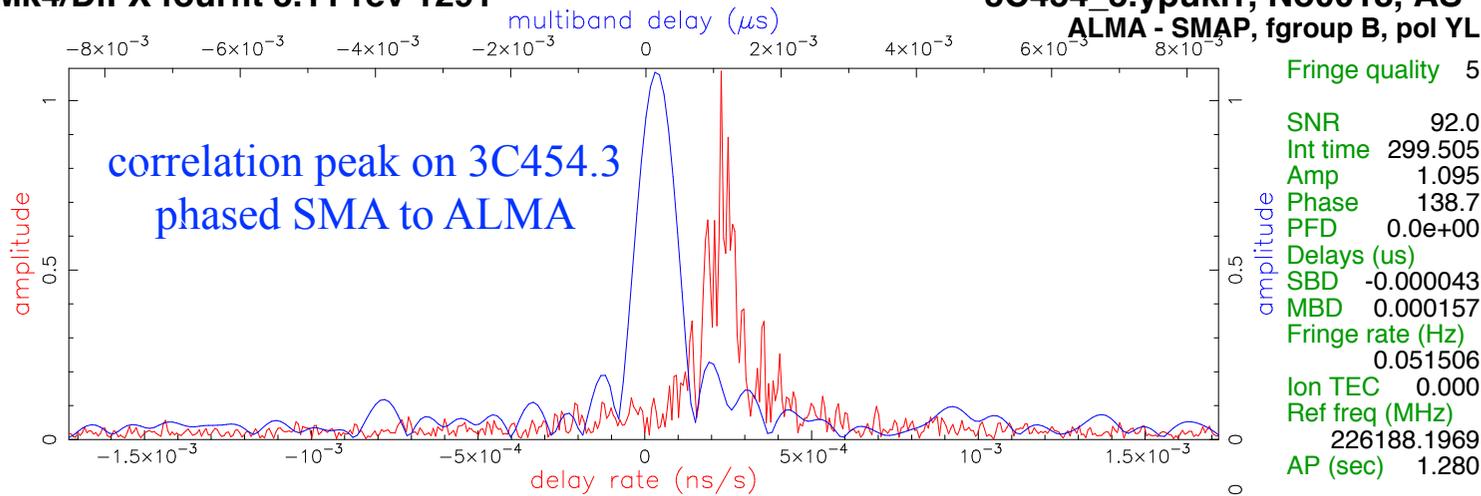
Primiani et al., JAI, 2016, in review

SWARM is EHT-ready

Phased ALMA to SMA Fringe, 22 Jan 2016
2015, 2016 annual campaigns observed and fringes verified.

Mk4/DiFX fourfit 3.11 rev 1291

3C454_3.ypukrr, No0018, AS
ALMA - SMAP, fgroup B, pol YL

correlation peak on 3C454.3
phased SMA to ALMA

Fringe quality	5
SNR	92.0
Int time	299.505
Amp	1.095
Phase	138.7
PFD	0.0e+00
Delays (us)	
SBD	-0.000043
MBD	0.000157
Fringe rate (Hz)	
	0.051506
Ion TEC	0.000
Ref freq (MHz)	
	226188.1969
AP (sec)	1.280

**Geoff Crew, Mike Tttus,
Roger Cappallo, Adam Deller,
ALMA phasing Geoff Crew and
Lynn Matthews, and many more!**

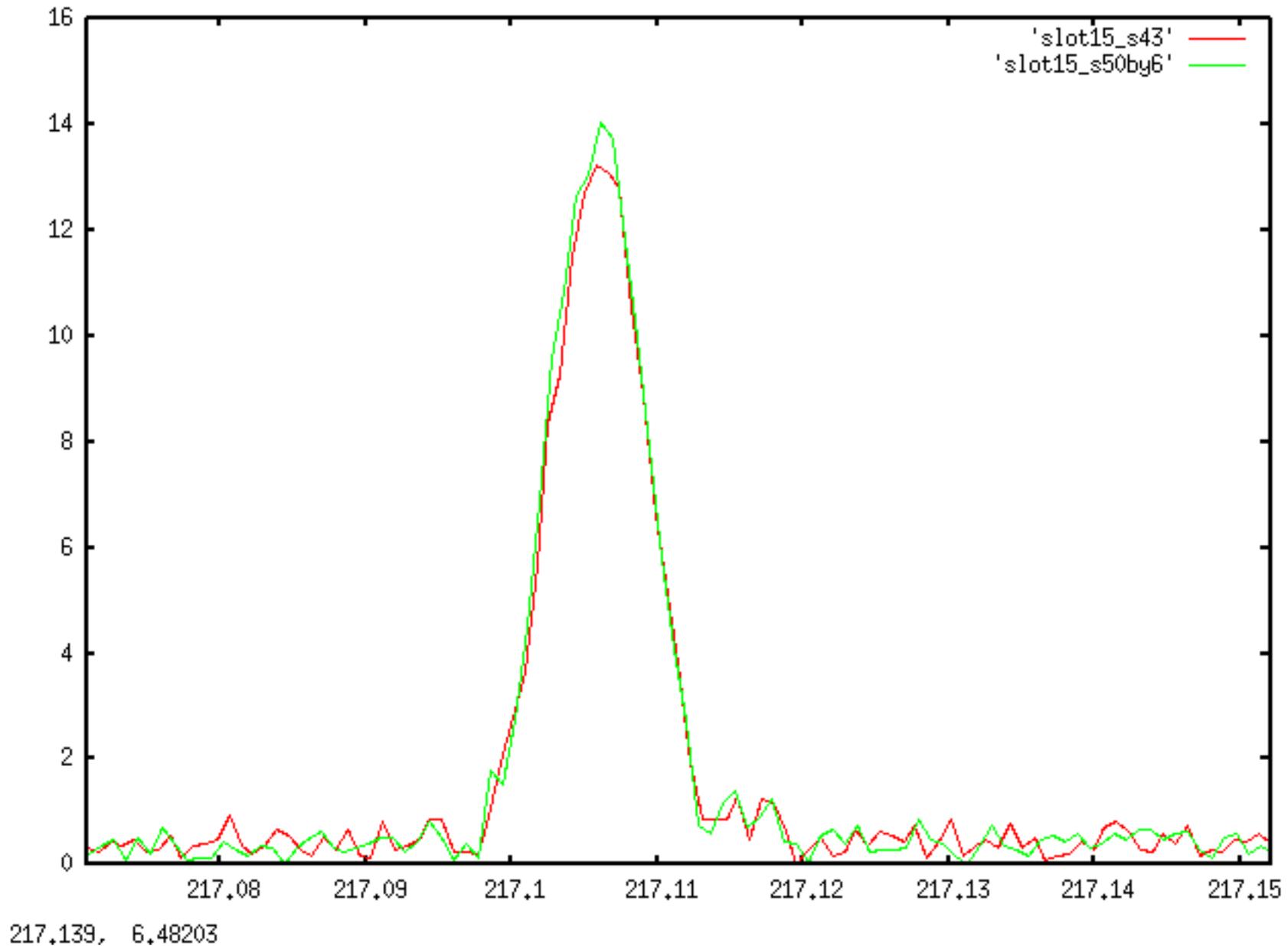SMA phasing efficiency on various sources, EHT campaign
4 April 2016
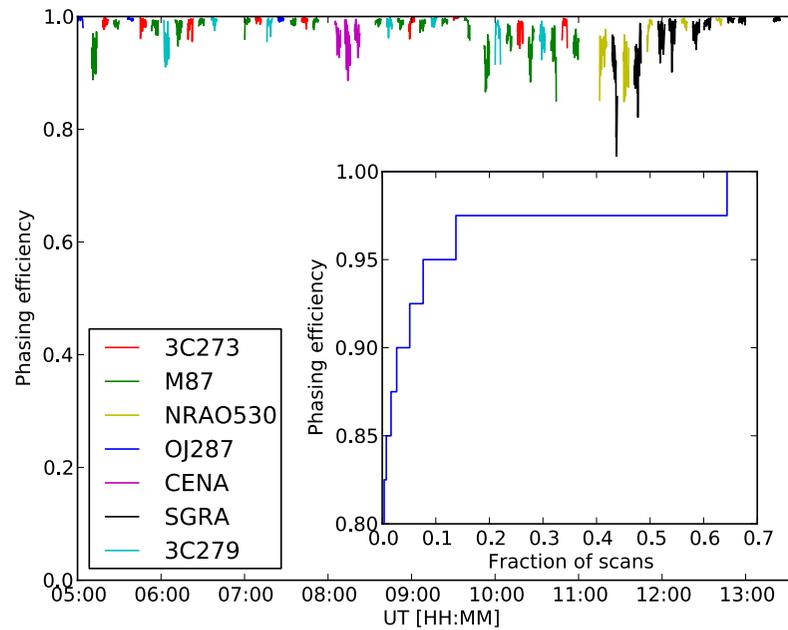
**A. Young, Primiani, K. Young,
Weintroub, et al., IEEE Phased
Array Conference, October 2016**

(talk by Keiichi Asada, this workshop, on EHT)

A 4-bit correlator is more efficient than 2-bit

SiO maser in R-Cas was used to measure the ratio of SWARM/ASIC SNR.

ASIC SiO line is red. SWARM line is green.
By measurement, SWARM SNR is 11 +/- 3% better

SMA's Future Upgrade: From 32 GHz to 56 GHz total BW
(14 GHz per pol per sideband; Grimes, et al., prior talk)

- Simply keep building until seven SWARM "quadrants"?
- That may the the fastest "time to science"
- Safe and conservative; however, rather unimaginative
- What is the rationale to stretch our in-house technology?

SMA's Future Upgrade: From 32 GHz to 56 GHz total BW

- Si   ts"?
- Th
- Sa   e
- W   gy?

North American ALMA Science Center

NORTH AMERICAN ARC
ALMA Regional Center

NRAO

Development Upgrades of the Atacama Large
Millimeter/submillimeter Array (ALMA)

Study Proposal Form

STUDY PROPOSAL TITLE:

DIGITAL CORRELATOR AND PHASED ARRAY ARCHITECTURES FOR UPGRADING ALMA

PRINCIPAL INVESTIGATOR: JONATHAN WEINTROUB

INSTITUTION: SMITHSONIAN ASTROPHYSICAL OBSERVATORY

Digital Correlator and Phased Array Architectures for upgrading ALMA

N.A. ALMA Development Study awarded to SAO
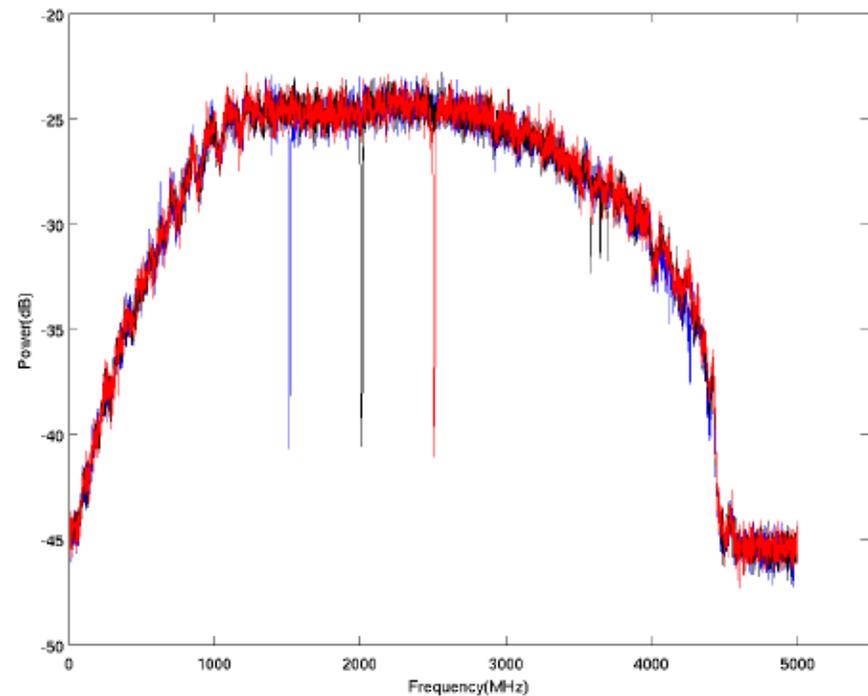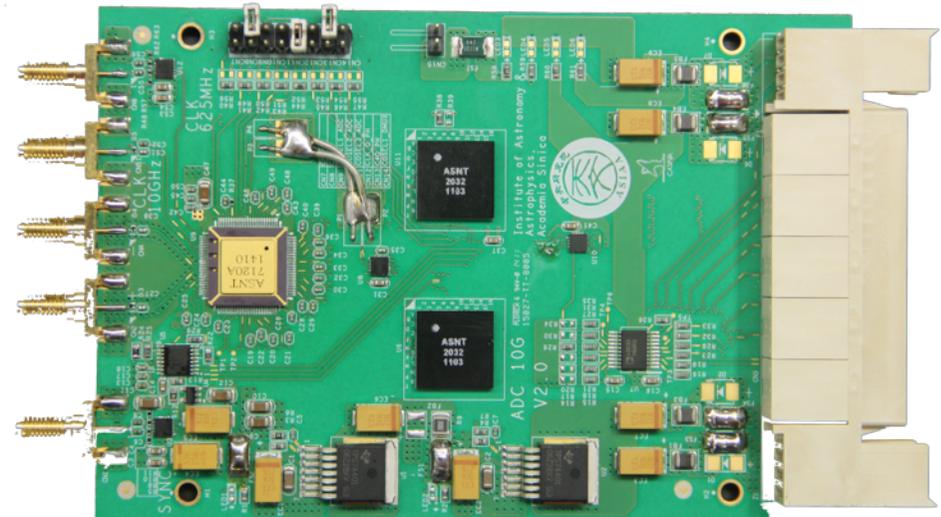Study team kick off meeting at CfA, 10, 11 May 2016

A 10 GSa/s single core CASPER ADC from ASIAA
based on Adsantec ANST7120A-KMA
Jiang, Yu & Guzzino (2016)
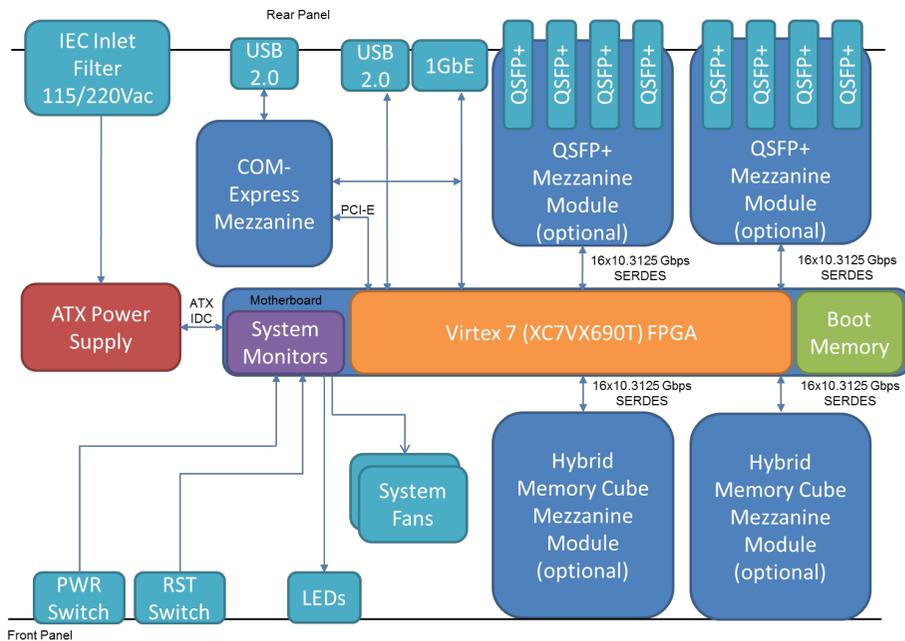

Homin Jiang, ASIAA, with 10 Gsps ADC, yesterday

Analog frequency response 0 to 5 GHz

SKARAB: SKA Reconfigurable Application Board
(designed for MeerKAT by Peralex, South Africa, based on Virtex7 VX690T)

Henno Kriel, MeerKAT DSP engineer & CASPERite, with SKARABs
August 2016, Pinelands, South Africa

Product Specifications:

SKARAB: SKA Reconfigurable Application Board
(designed for MeerKAT by Peralex, South Africa, based on Virtex7 VX690T)

ADSANTEC

ASNT

Ultra High-Speed Mixed Signal ASICs

Advanced Science And Novel Technology Company, Inc.
27 Via Porto Grande, Rancho Palos Verdes, CA 90275

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www.adsantec.com

ASNT7122-KMA
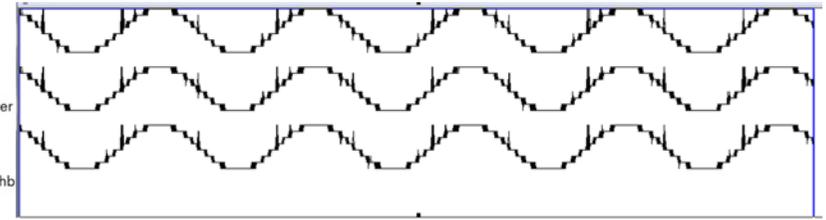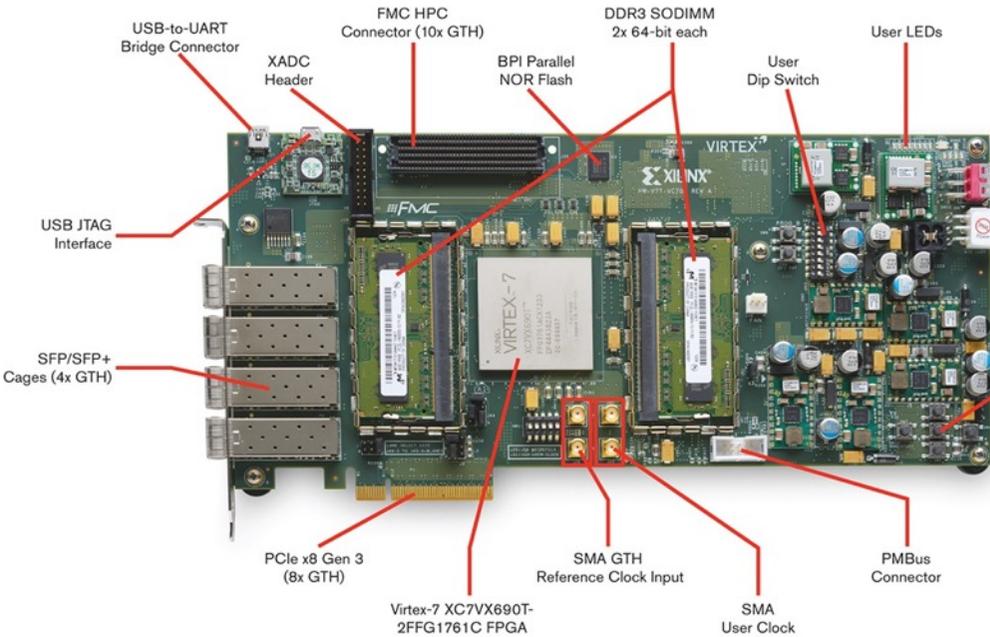## $15GS/s$, 4-bit Flash Analog-to-Digital Converter with HS Outputs

- $20GHz$ analog input bandwidth
- Selectable clocking mode: external high-speed clock or internal PLL with external reference clock
- Broadband operation in external clocking mode: DC-$15GS/s$
- On-chip PLL with a central frequency of $10GHz$
- Selectable on-chip PRBS 2^{15}-1 generator for output data scrambling
- Differential CML input clock buffer and output data and clock buffers
- Differential linear data input buffer
- LVDS input reference clock buffer
- Selectable on-chip digital-to-analog converter for self-testing

Front Panel

Product Specifications:

SAO 20 GS/s ADC based on Hittite HMCAD5831LP9BE, single core

(Weintroub and Raffanti, ISSTT, 2015)

USB-to-UART Bridge Connector
XADC Header
FMC HPC Connector (10x GTH)
BPI Parallel NOR Flash
DDR3 SODIMM 2x 64-bit each
User Dip Switch
User LEDs
Power Switch
12V Power
User Pushb
USB JTAG Interface
SFP/SFP+ Cages (4x GTH)
PCIe x8 Gen 3 (8x GTH)
SMA GTH Reference Clock Input
Virtex-7 XC7VX690T-2FFG1761C FPGA
SMA User Clock
PMBus Connector

VC709 Xilinx V7 Evaluation Board
bargain basement price: $4995

"sparkle codes" ~ 1 in 1000 frequency

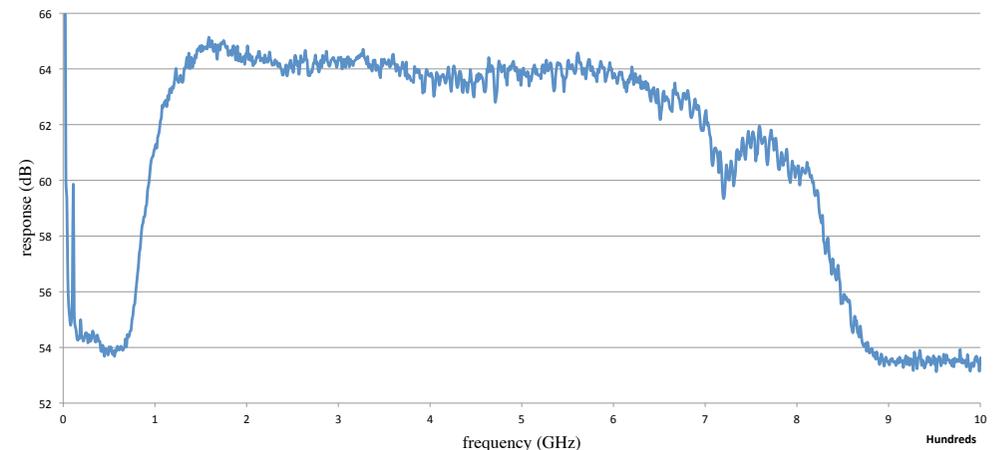persistence display

single event

SERDES Transceivers:
GTP, GTX, GTH, GTZ

GTH features:

- 7 tap decision feedback equalizer (DFE) vs 5-tap for GTX

- Rx reflection cancellation

- In the Tx, the "Phase Interpolator PPM Controller" which allows fine-grain adjustment of the Tx phase

2 to 8.2 GHz Noise passband

power spectrum of 3-bit sampled noise



response (dB) vs frequency (GHz)

The best way to predict the future is to create it
Abraham Lincoln

- All goals for SWARM set at project inception are met

- Engineering decisions made at the outset are validated:
  - Quad-Core wideband ADC technology for science-quality data
  - Full featured FPGA logic with ability to project required resources
  - Fit in FPGA a hi-res FX correlator with EHT phasing and recording
  - And more . . .

- The future is bright:
  - Quad4 build will complete 32 GHz SWARM this calendar year…
  - …then develop and access yet wider band ADC, FPGA technology…
  - …apply our expertise to upgrade ALMA…
  - …and build skills and capacity in DSP for broad application!

Questions?
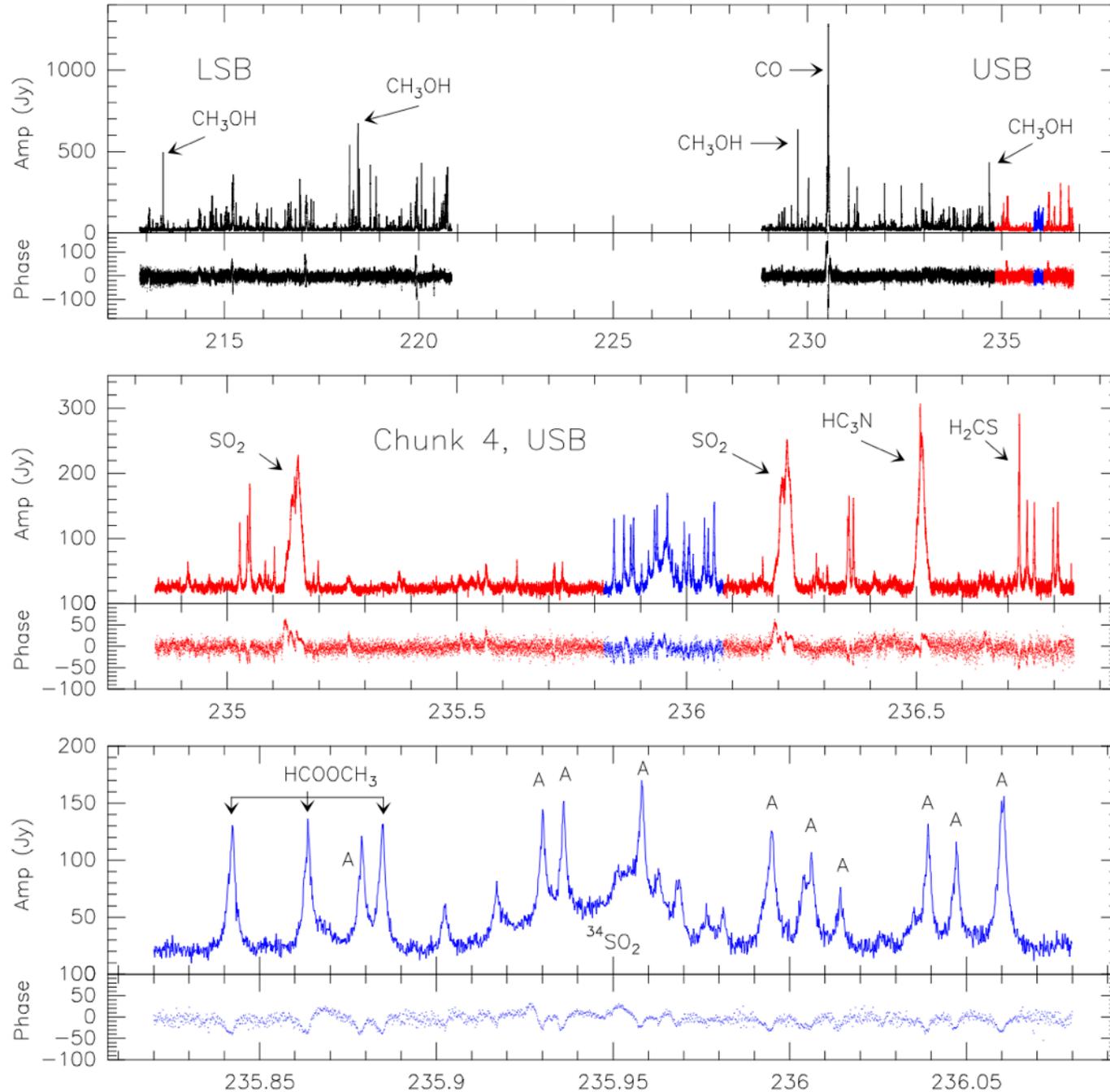
Orion BN/KL line forest plot from Primiani et al., JAI, 2016, in review

Questions?

"With correlator performance having gone up by a factor of 922,000 over the last 30 years, its only fair that correlator design engineers' salaries should have gone up by a similar factor"

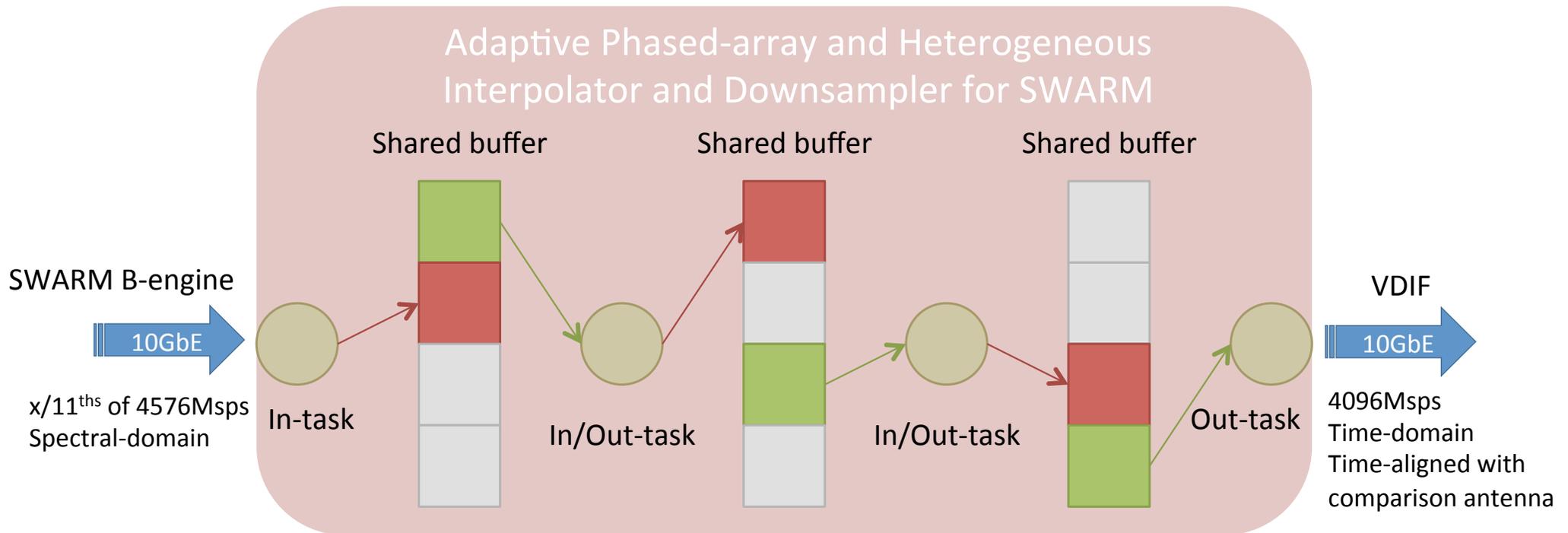Ray Escoffier, leader of N.A. ALMA correlator team, over a decade ago

Questions?
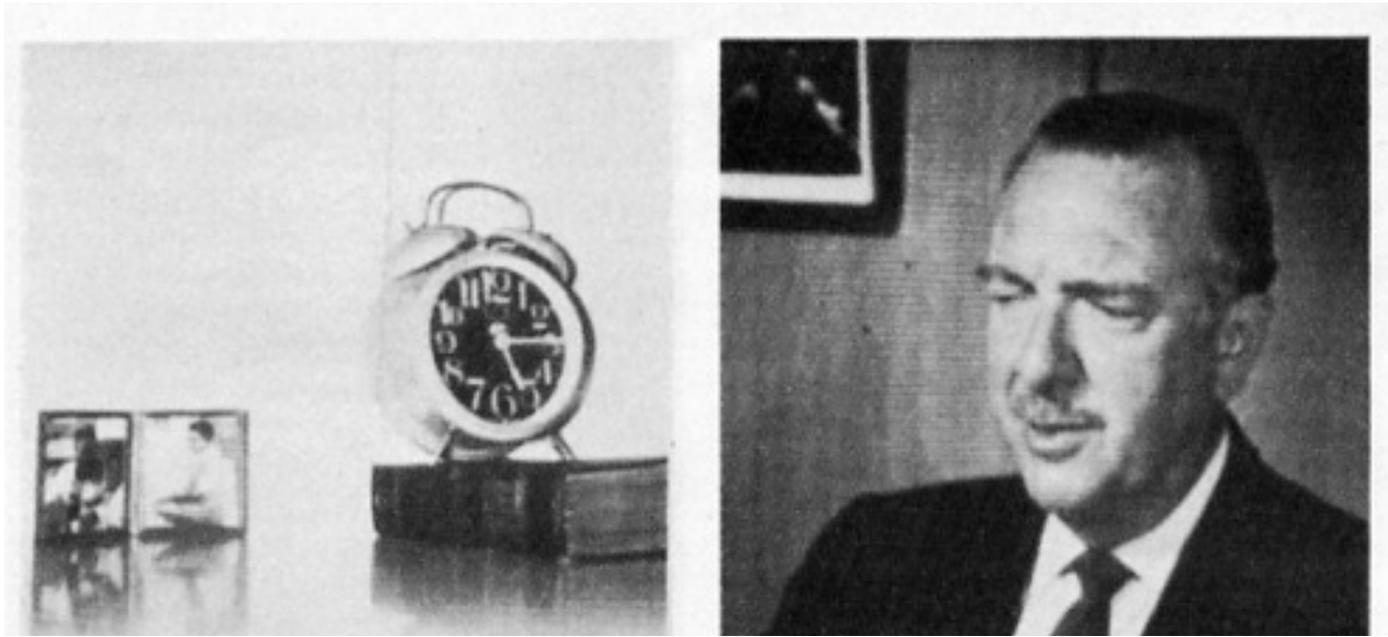

xkcd.com

supplementary material
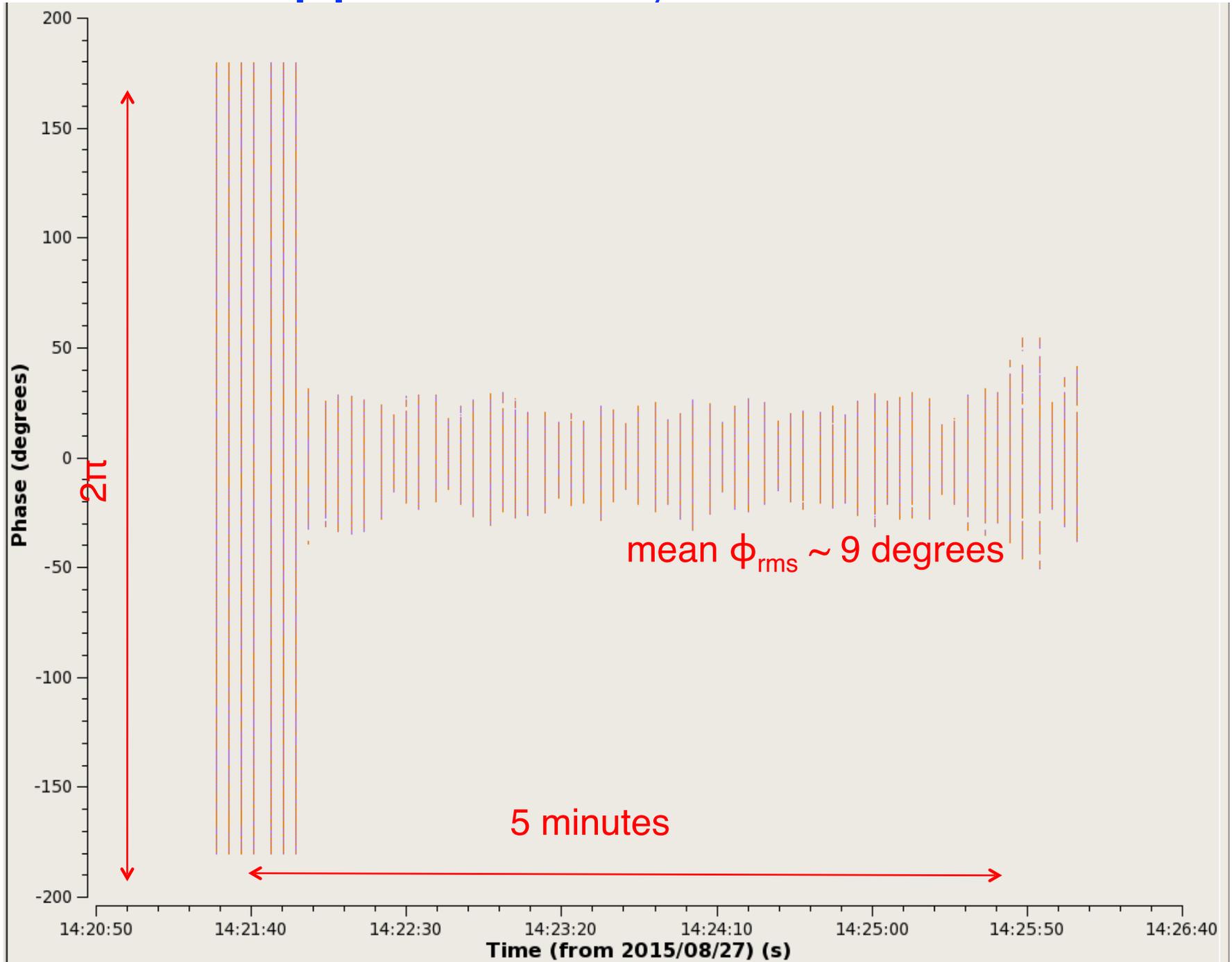
APHIDS Interpolation and inversion software

- **APHIDS is GPU-accelerated post processing software built on #| by Dave MacMahon,** developed primarily by *André Young* and Katherine Rosenfeld, with help from Lindy Blackburn and Rurik Primiani.

- **https://github.com/david-macmahon/hashpipe)**

- APHIDS converts spectral-domain SWARM data to the equivalent time-domain R2DBE data, which includes resampling, filtering, and frequency conversion.

- GPU acceleration means the ultimate goal of real-time on-the-fly "may be possible".

The Importance of Phase

Oppenheim
& Lim, 1981